IN THE CLAIMS:

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Please amend claims 1, 2, 3, 4, 6, 7, 8, 10 and 11 as follows:

1. (currently amended) A content addressable memory comprising a CAM control logic unit [(1)] and a plurality of cells [(10)] connected in a chain, each cell comprising:

a memory block [(12)] coupled to a common address bus [(ADD)];

a comparator [(14)] coupled to a common data bus [(DATA)] and to the data interface of the memory block [(12)];

B3 a switch for [switching means (15)] coupling the data interface of the memory block with the data bus, and;

a logic block [(13)] including a Match flip-flop [(16)]:

the memory being operable:

in a Search phase to serially match a sequence of words on the common data bus [(DATA)] with the contents of a sequence of addresses in the memory blocks [(12)] of the cells [(10)] , the logic block being arranged for cumulatively storing the results of the matching as the matching proceeds; and

in an Access phase, to render the cells matched in the Search phase serially available for access via the common address and data buses [(ADD and DATA)].

2. (currently amended) A content addressable memory according to claim 1 wherein each cell [contains] includes a memory block [(12)], a logic block [(13)], a comparator [(14)], and a bidirectional switch [(15)].

3. (currently amended) A content addressable memory according to claim 1, [implemented on] wherein an integrated circuit chip carries the CAM and plural cells.

4. (currently amended) A content addressable memory according to claim 3 wherein several [such] of the chips [can be] are chained.

5. (original) A content addressable memory according to claim 4 wherein each chip includes a control unit which can be disabled.

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6. (currently amended) A content addressable memory according to claim 1 including a MASK bus input [which determined] for determining which bits of the words of the sequence of words are used for matching in the Search phase.

7. (currently amended) A content addressable memory according to claim 1 including a return line from the end of the chain of cells back to the CAM control unit [11 which changes] for changing state [when] in response to all Match flip-flops in the chain [have] having been accessed.

8. (currently amended) A method of operating a content addressable memory according to claim 1 [wherein] comprising the steps of choosing a standard byte address [is chosen] in all data blocks and including a byte different from the inactive state of the data bus [is included] in that address in every data block.

9. (previously amended) A method of operating a content addressable memory according to claim 1 wherein each cell is divided into a plurality of distinct data blocks.

10. (currently amended) A method of operating a content addressable memory according to claim 1 wherein a plurality of cells are combined into an extended data block with all cells of the block [containing] including corresponding key fields.

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11. (currently amended) A method of operating a content addressable memory according to claim 1 [wherein] further including choosing a standard byte address [is chosen] in all data blocks and [filled] filling the data blocks with one data value if the data block in that cell is valid and another data value if the data block in the cell is cleared [ie invalid].

12. (previously cancelled)